

DFW  
Dkt. 2271/71388

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Junji ICHIMIYA

Serial No.: 10/701,249

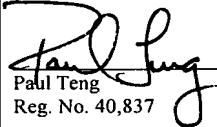
Group Art Unit: 2825

Date Filed: November 4, 2003

Examiner: Tuyen To

For: LAYOUT DESIGN METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT,  
AND SEMICONDUCTOR INTEGRATED CIRCUIT

I hereby certify that this correspondence is being deposited this date with the U.S. Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

  
Paul Teng

Reg. No. 40,837

December 1, 2005

Date

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Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**AMENDMENT**

Sir:

This Amendment is submitted in response to the Office Action dated September 8, 2005 in connection with the above-identified application.

**Amendment to the Title** begins on page 2 of this paper.

Amendments to the Claims are reflected in the **Listing of Claims** section which begins on page 3.

**Remarks** begin on page 7 of this paper.